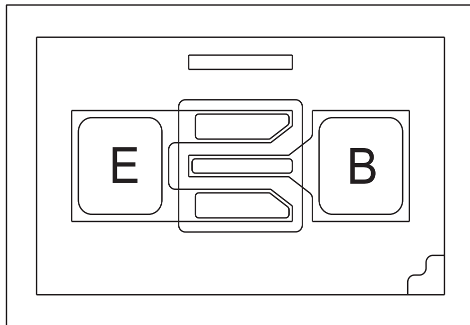
Central™
Semiconductor Corp.

PROCESS CP207
Small Signal Transistor
NPN - Saturated Switch Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	9.0 x 14 MILS
Die Thickness	8.0 MILS
Base Bonding Pad Area	3.1 x 2.9 MILS
Emitter Bonding Pad Area	3.1 x 2.9 MILS
Top Side Metalization	Al - 13,000Å
Back Side Metalization	Au - 6,000Å

GEOMETRY



BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER
93,430

PRINCIPAL DEVICE TYPES
2N2369A
CMPT2369

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R3 (16-August 2006)

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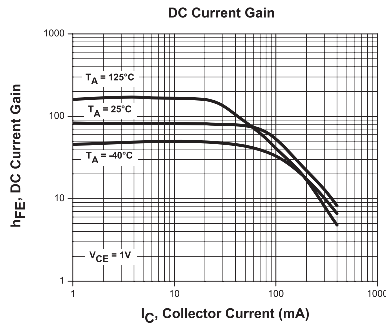
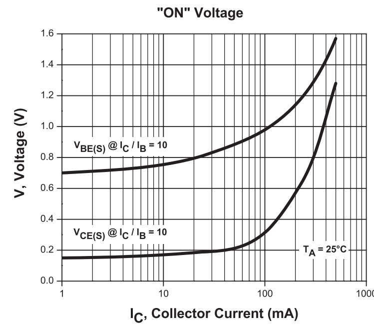
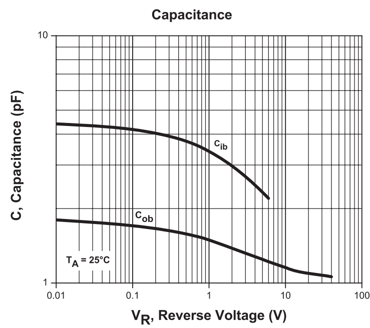
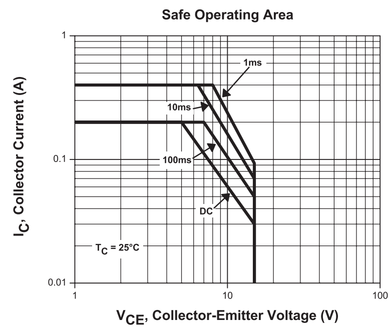
PROCESS CP207

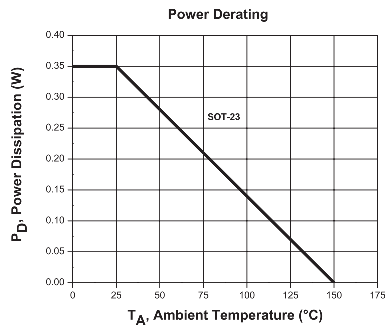
Typical Electrical Characteristics

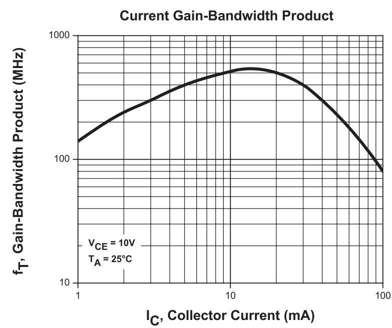












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